

Automotive Electronics

Product Information

E-Ray IP Module



BOSCH
Invented for life



The FlexRay Communication Controller – IP Module

Customer benefits:

- ▶ Full FlexRay IP-Module including Message Handling
- ▶ Most widely used FlexRay IP Module
- ▶ 100% successfully conformance tested
- ▶ Driver support by established companies

Features

- ▶ Conform with protocol specification v2.1
- ▶ Data rates of up to 10 MBit/s on each channel
- ▶ Configurable Message RAM supports
 - Up to 128 Message Buffers
 - Up to maximum payload of 254 Bytes
 - Different payload lengths possible
 - One configurable Receive FIFO
 - Each Message Buffer can be configured as Receive Buffer, as Transmit Buffer or as part of the Receive FIFO
- ▶ Host access to Message Buffers via Input and Output buffer
- ▶ Filtering for Frame ID, Channel ID, and Cycle Counter
- ▶ Network Management supported
- ▶ Maskable module interrupt
- ▶ 8/16/32-bit generic CPU Interface, connectable to customer-specific Host CPUs

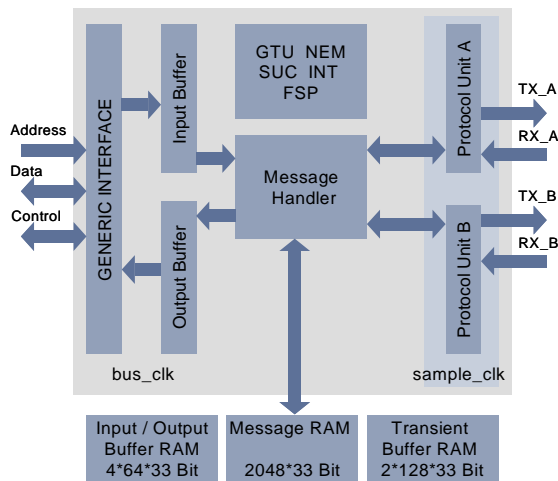
General description

The E-Ray Module is the FlexRay Communication Controller IP-module from Bosch that can be realized as a stand-alone device, as part of an ASIC or as a FPGA. It performs communication according to the FlexRay protocol specification v2.1.

For communication on a FlexRay network, individual message buffers with up to 254 data bytes are configured. The message storage consists of a single-ported Message RAM that holds up to 128 Message Buffers. All functions concerning the handling of messages are implemented in the Message Handler. Those functions are the acceptance filtering, the transfer of messages between the two FlexRay Protocol Controllers and the Message RAM, maintaining the transmission schedule as well as providing message status information.

The register set of the E-Ray module can be accessed directly by an external CPU via the modules Host interface. These registers are used to control/configure/monitor the FlexRay Protocol Controllers, Message Handler, Global Timing Unit, System Universal Control, Frame and Symbol Processing, Network Management, Interrupt Control, and to access the Message RAM via Input / Output Buffer. The E-Ray Module can be connected to a wide range of customer-specific Host CPUs via its 8/16/32-bit Generic CPU Interface.

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Block functions and size

Generic Interface (GIF)

The 8/16/32-bit Generic CPU Interface is adaptable for the connection to a wide range of customer-specific CPUs.

Input Buffer (IBF) & Output Buffer (OBF)

Store two complete message buffers each for transfer to / from the Message RAM.

Message Handler (MHD)

Controls data transfers between Input / Output Buffer and Message RAM, and between the two FlexRay Protocol Controllers and the Message RAM.

FlexRay Protocol Unit (PRT A,B)

The FlexRay Protocol Units consist of Shift Register and FlexRay Protocol FSM. They are connected to Transient Buffer RAMs for intermediate message storage.

Message RAM

Single-ported RAM that stores the FlexRay message buffers together with the related configuration data.

Global Time Unit (GTU)

Supplies microtick (μT) / macrotick (MT), fault tolerant clock synchronization, cycle counter, and timing control of static / dynamic segment.

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System Universal Control (SUC)

Controls Wakeup, Startup, and (Re)Integration of the node.

Frame and Symbol Processing (FSP)

Checks the correct timing of frames and symbols, tests the syntactical and semantical correctness of received frames.

Network Management (NEM)

Handling of the Network Management Vector.

Interrupt Control (INT)

Controls generation of module interrupts.

Approximate size of E-Ray IP module for ASIC design

E-Ray	110,000 gates
Message RAM	8.25 kbytes

Approximate size of E-Ray IP module for Altera FPGAs

E-Ray	12,780 ALUTs + 23 M4Ks RAM
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Approximate size of E-Ray IP module for Lattice FPGAs

E-Ray	19,040 LUT4s + 920 LUT4s RAM + 8 EBRs RAM
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Deliverables for ASIC design

- ▶ Well documented VHDL source code
- ▶ AHB customer interface example
- ▶ VHDL test bench
- ▶ User's Manual (programmer's view)
- ▶ Module Integration Guide (designer's view)
- ▶ Application Examples

Deliverables for FPGA design

- ▶ Altera encrypted VHDL source code or Lattice synthesized core netlist
- ▶ Source code of Altera Avalon bus interface for Altera or Wishbone interface for Lattice
- ▶ E-Ray User's Manual and Specification
- ▶ FPGA Integration Guide

Supported FPGA families

- ▶ Altera Cyclone and Stratix series
- ▶ Lattice ECP and XP series