BOSCH
Invented for life

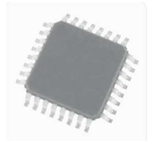
GTM

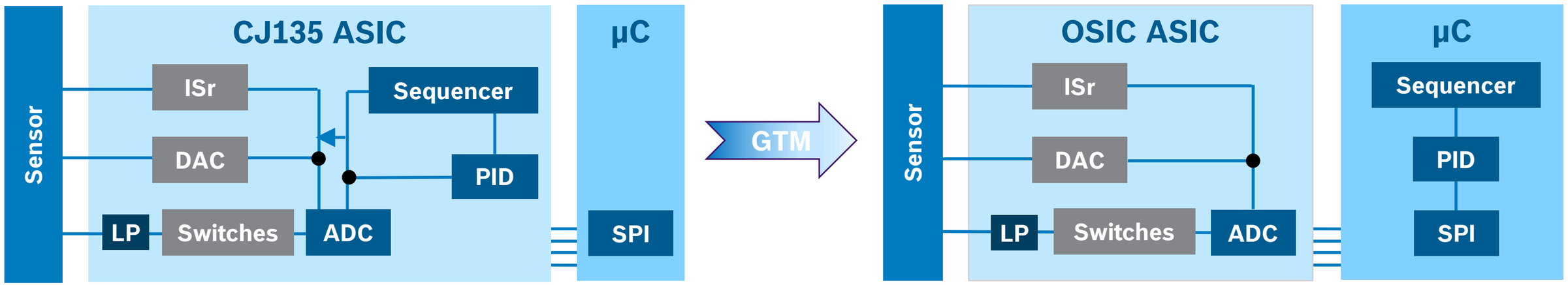
- The technology of an ASIC should be optimized for the intended use case
  - Including processing units and memory into a mixed signal ASIC can be in conflict with the analog functions of the ASIC
  - The ASIC function is fixed to the requirements existing at the date of design
  - Changes of functions in the ASIC HW are not possible without metal change

- The technology of a micro controller is optimized for calculations and digital processing
  - Use the µC for computing and storage of data
  - Use GTM Multi Channel Sequencer (MCS) for time critical actions
  - By separating calculation functions and digital processing from analog functions, the ASIC can be designed in an optimized semiconductor process

The technology of an ASIC should be optimized for the intended use case

Comparison CJ135 to OSIC (Oxygen Sensor ASIC)





New partitioning between µController and Mixed Signal IC enables system and cost benefit

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Comparison CJ135 to OSIC (Oxygen Sensor ASIC)

- CJ135:
  - Switches, Current supply and ADC
  - Nernst voltage controller (Governor)
  - Selectable Sequences / Program in Metal mask
  - CPU and DSP
  - Communication using Registers and RAM
  - Housing TQSP32epad
- OSIC:
  - Switches, Current supply and ADC
  - -
  - Fix sequence identical for each measurement
  - Simple logic
  - Communication using single shift Register
  - Housing SO14

Significant Hardware simplification enables system and cost benefit

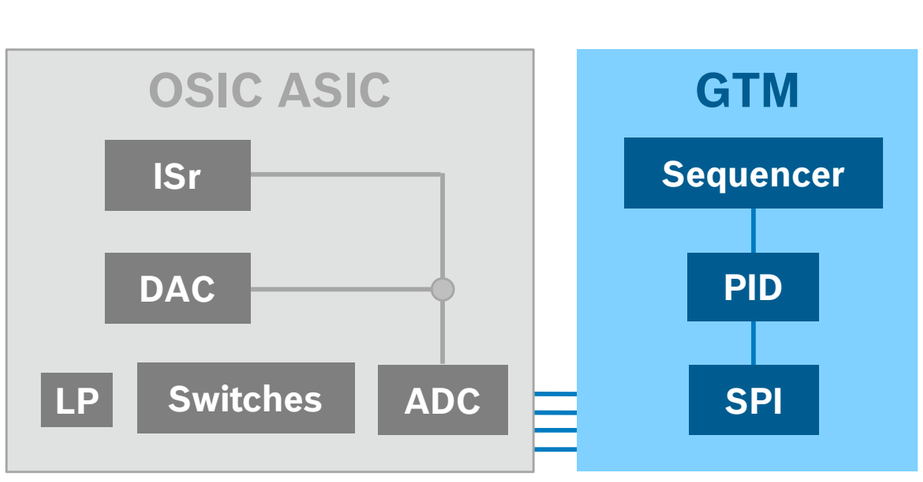
- CJ135 µController software:
  - Code implemented for ST and IFX controllers
  - -
  - -
  - -
  - Standard SPI
  - Update of control data each 10 ms
  - 60 Measurement values each 10 ms
  - Block transfer 10 ms
  - -

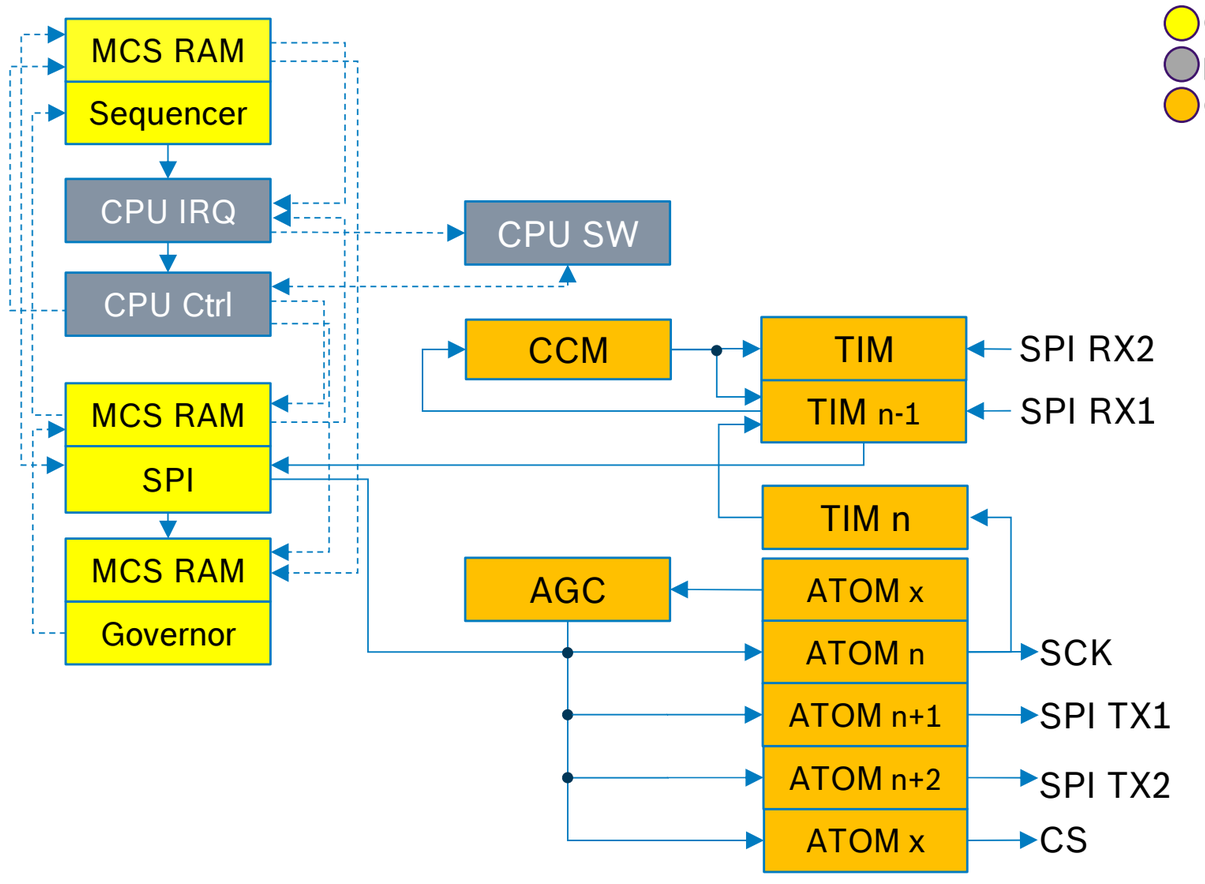
- OSIC µController software :
  - Code implemented for ST and IFX controllers
  - Sequencer **GTM MCS** program
  - Nernst voltage controller **GTM MCS** program
  - SPI emulation **GTM MCS** program
  - **GTM MCS** Software and GTM Timer Cells
  - Update of control data each 71.2 µs
  - 140 Measurement values in 10 ms
  - Single transfer 71.2 µs
  - **GTM MCS** Code identical for GTM3.1 and GTM 4.x

Increased flexibility of functions moved to µController

Oxygen Sensor control partitioning (GTM)

- OSIC solution Software:
  - GTM Timer Cells for SPI signals
  - Sequencer @ GTM MCS program
  - Nernst voltage controller @ GTM MCS program
  - SPI emulation @ GTM MCS program





Partitioning OSIC control in GTM MCS and Timer Cells

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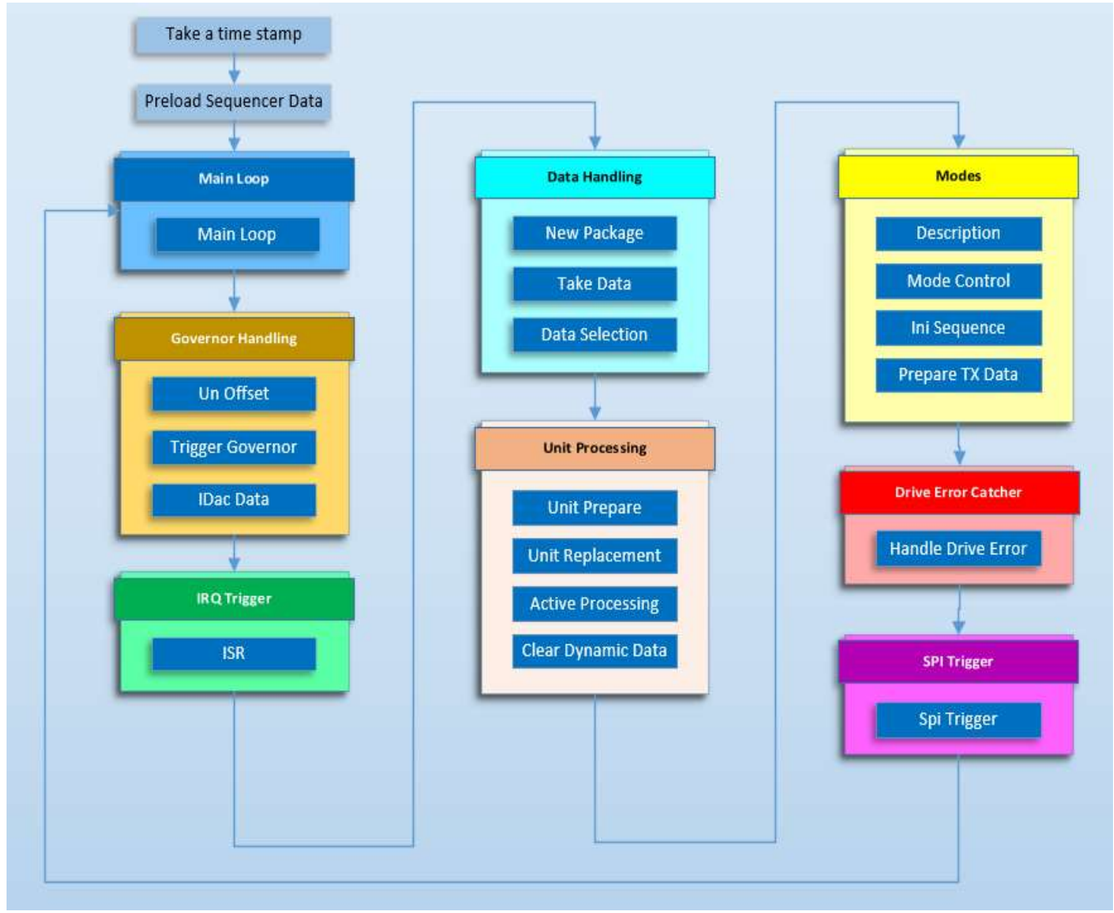
Oxygen Sensor control partitioning (Sequencer)

- GTM MCS Sequencer
  - Generate the Timing
  - Data selection out of MCS RAM stored values
  - Implement Mode handling and active Sequences
  - Error logging
  - Prepare SPI (TX) data
  - Prepare Nernst Voltage controller data
  - Trigger SPI TX
  - Trigger Nernst voltage controller
  - Trigger Interrupt



GTM MCS Sequencer on µController enables high flexibility

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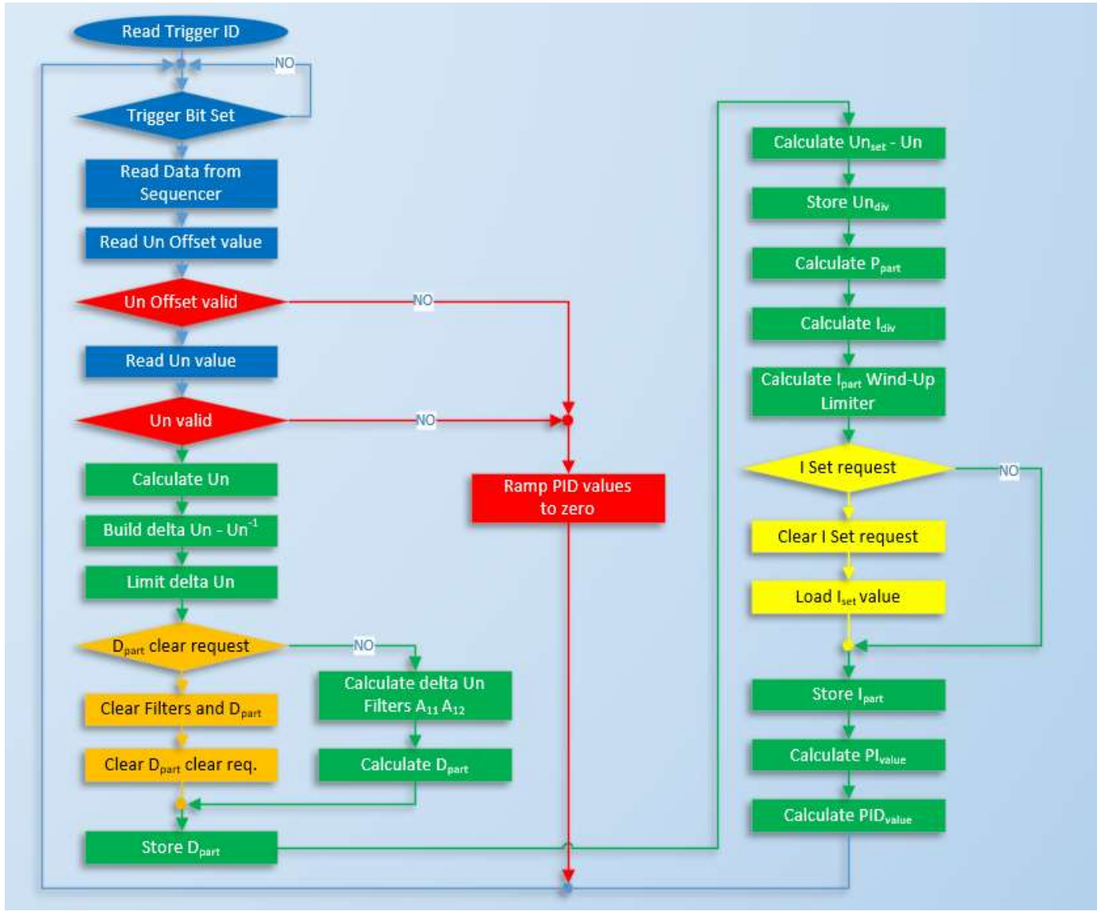
Oxygen Sensor control partitioning (Governor)

- GTM MCS Nernst Voltage Controller (Governor)
  - Triggered from Sequencer
  - Failure Handling
  - Calculate Nernst voltage Setpoint
  - Calculate D-Filter, PID
  - Trigger DMA transfer



GTM MCS Governor on µController reduces ASIC complexity

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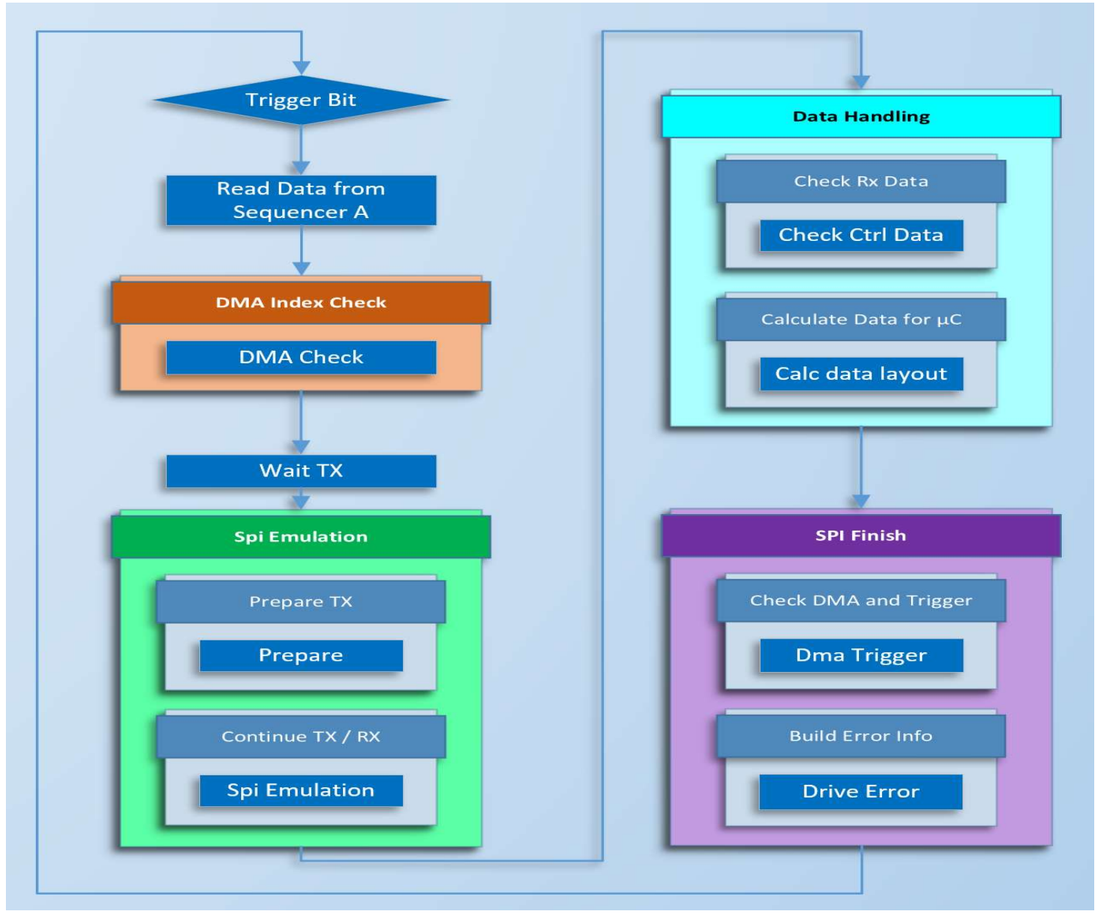
Oxygen Sensor control partitioning (SPI Emulation)

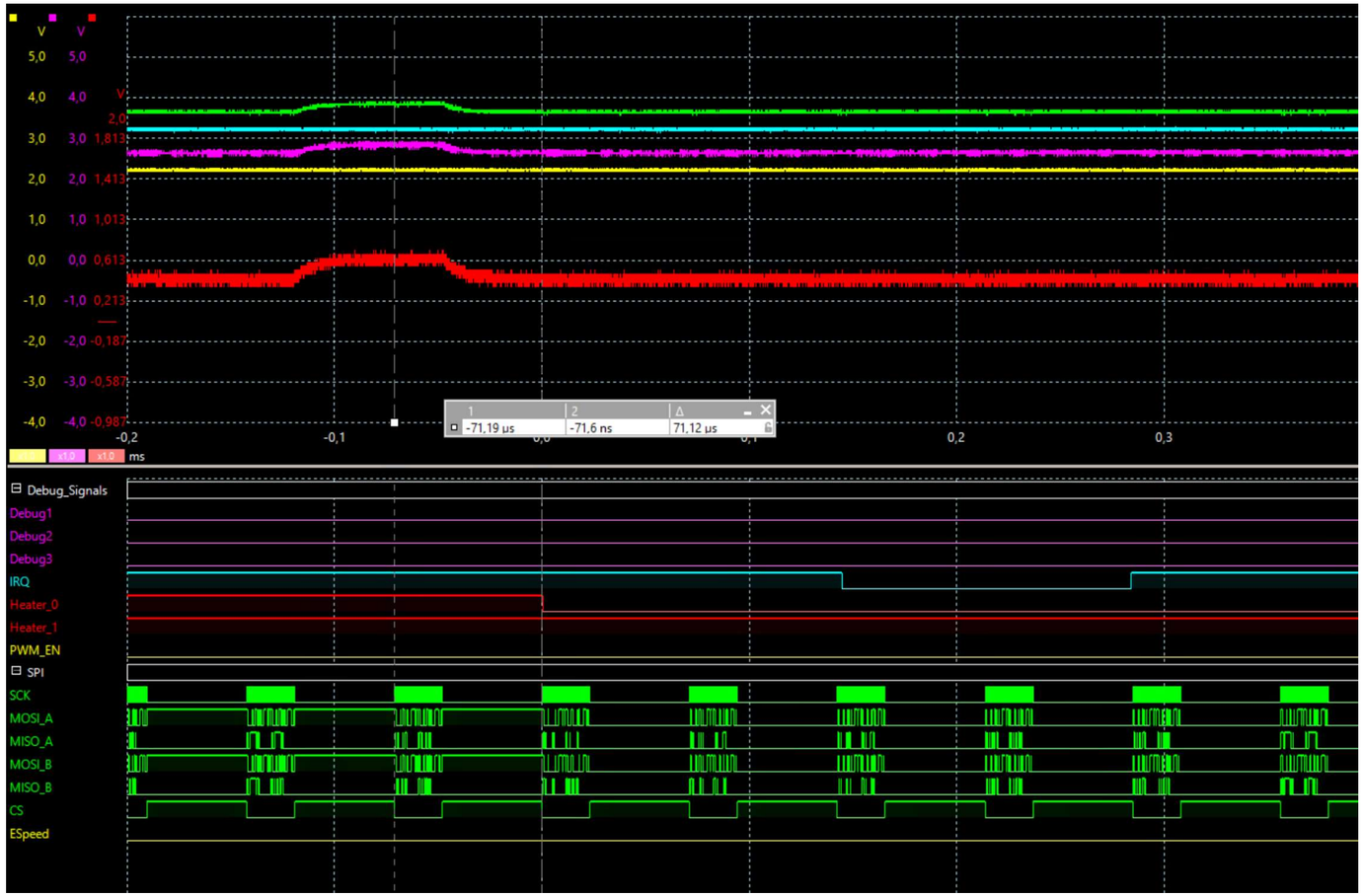
- GTM MCS SPI Emulation
  - Triggered from Sequencer
  - DMA Monitoring
  - TX / RX Data transfer
  - Data evaluation
  - Data optimized for CPU access
  - Failure Handling
  - Trigger DMA for transfer of Data to the CPU



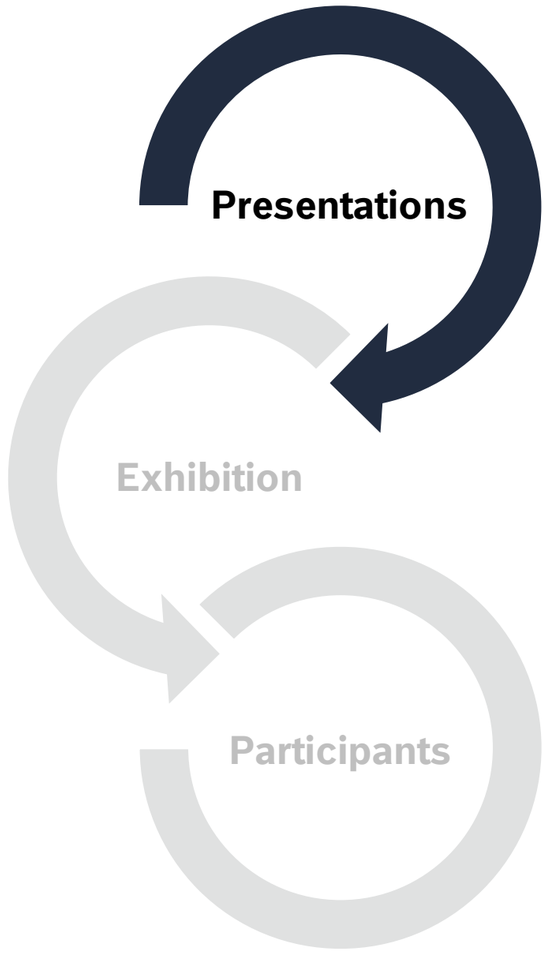
GTM MCS fast SPI Emulation on µController is mandatory

Oxygen Sensor control partitioning (SPI)

- SPI Communication
  - Clock 4.17 MHz
  - CS lead / trail 50ns
  - Daisy Chain 2 x 48 Bit (2 OSIC = 96 Bit)
  - Error detecting 8 Bit
  - Payload 32 Bit
  - Manufacturer data 8 Bit
  - Rx/Tx Time 23 µs
  - Sequencer cycle 71.2 µs
  - Governor calculation 30 µs



GTM MCS SPI Emulation (fast speed communication)



THANK YOU!